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10/603,746	06/26/2003	Jeom-Jin Chang	1572.1150	3810

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EXAMINER	
WYSZYNSKI, AUBREY H	

ART UNIT	PAPER NUMBER
2134	

DATE MAILED: 12/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,746	CHANG, JEOM-JIN	
	Examiner	Art Unit	
	Aubrey H. Wyszynski	2134	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 are pending.

Response to Amendment

2. Claim 14 has been amended to over come the 35 U.S.C. §112, 2nd ¶ rejection. Therefore, the rejection is withdrawn.

Response to Arguments

3. Applicant's arguments filed 9/25/06 have been fully considered but they are not persuasive.

4. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, applicant suggests Challener teaches the advantages of performing an operation with no power and the selection between BIOS programs taught by Lin requires power to be on. However, the Challener reference is used to teach the limitation of "byte-adding a user password and a product serial number", (col. 8, lines 33-37; col. 6, lines 13-17; and fig. 5, #607). In response to applicant's argument that there is no motivation to combine the

Challener and Lin references because they are at odds with each other, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

5. Applicant argues (page 5, ¶7) that Challener enables writing when the stored and calculated checksum values are equal. However, the examiner is not relying on Challener for teaching enabling writing when the stored and calculate checksums are equal. The examiner is relying on Challener for teaching "byte-adding a user password and a product serial number of a BIOS ROM" (col. 8, lines 33-37; col. 6, lines 13-17; and fig. 5, #607). This teaching of Challener would have been obvious to one of ordinary skill in the art to combine with the teachings of Lin, wherein Lin discloses enabling writing to the BIOS ROM when the stored and calculated checksum values are equal. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Lin with the device of Challener to store a checksum value calculated by adding a user password and serial number in order to secure and strengthen the password in the BIOS using a serial number as derived secret as taught by Challener, (col. 8, lines 35-37).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 5-7, 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Challener et al., USPN 6,748,544 and further in view of Lin, USPN 6,892,323.

Regarding claim 1, Lin discloses a method of improving BIOS (Basic Input Output System) security of a computer system (col.1, lines 13-17) and storing a check sum value (col. 6, lines 20-23). Lin lacks or does not expressly disclose byte-adding a user password and a product serial number. However, Challener discloses byte-adding a user password and a product serial number (col. 8, lines 33-37 & col. 6, lines 13-17 and fig. 5, #607). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Lin with the device of Challener to store a checksum value calculated by adding a user password and serial number in order to secure and strengthen the password in the BIOS using a serial number as derived secret as taught by Challener, (col. 8, lines 35-37). Lin further discloses comparing the stored check sum value with a check sum value calculated by byte-adding an inputted password and the product serial number of the BIOS ROM (col. 6, lines 20-23); and enabling writing to the BIOS ROM when the stored check sum value and the calculated check sum value are equal (col. 6, lines 22-28 and fig. 3, #206).

Regarding claim 5, Lin further discloses comprising: setting up a memory-mapped input/output region assigned as a BIOS writing protection region of a chipset having a GPIO (General Purpose Input Output) function as an input/output trap region and enabling an input/output trap (col. 2, lines 17- 26); allowing an event disabling a BIOS writing protection during operation of the computer system to occur (fig. 3, #202); setting up the input/output trap as disabled (col. 6, lines 5-20); determining the product serial number (Challener, col. 6, lines 13-17) of the BIOS ROM (col. 6, lines 20-23); allowing a user to input the inputted password when the product serial number is not a default value in manufacturing and calculating a check sum value by byte-adding the inputted password and the product serial number (Challener col. 8, lines 33-37 & col. 6, lines 13-17 and fig. 5, #607).

Regarding claim 6, Lin further discloses comprising: enabling the input/output trap after enabling writing to the BIOS ROM (fig. 3, #202 and #206).

Regarding claims 7 and 11, Lin lacks or does not expressly disclose displaying an error message. However, Challener discloses displaying an error message when the product serial number is a default value in manufacturing, or when the check sum values (Lin, col. 6, lines 20-23) are not equal (fig. 4, #517). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Lin with the device of Challener to display an error message when the checksums do not match in order to notify the user the access in invalid, as taught by Challener (fig. 4,

#517).

Regarding claim 13, Lin discloses a machine-readable medium that provides instructions, which, when executed by a machine, cause the machine to perform operations of improving BIOS (Basic Input Output System) security of a computer system (col.1, lines 13-17). Lin lacks or does not expressly disclose byte-adding a user password and a product serial number. However, Challener discloses byte-adding a user password and a product serial number (col. 8, lines 33-37 & col. 6, lines 13-17 and fig. 5, #607). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Lin with the device of Challener to store a checksum value calculated by adding a user password and serial number in order to secure and strengthen the password in the BIOS using a serial number as derived secret as taught by Challener, (col. 8, lines 35-37). Lin further discloses comparing the stored check sum value with a check sum value calculated by byte-adding an inputted password and the product serial number of the BIOS ROM (col. 6, lines 20-23); and enabling writing to the BIOS ROM when the stored check sum value and the calculated check sum value are equal (col. 6, lines 22-28 and fig. 3, #206).

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Challener as applied to claim 1 above, and further in view of Cromer et al, US Patent Application Publication 2002/0120845.

Regarding claim 2, Lin in view of Challener discloses the method of improving BIOS security according to claim 1. Lin lacks or does not expressly disclose determining if the user password is set up on a POST. However, Cromer discloses wherein the storing the check sum value comprises: determining if the user password is set up on a POST (Power On Self Test) (¶[0020-0021]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Lin in view of Challener with the device of Cromer to determine of the password is set up in POST in order to authenticate the requester of the BIOS update by retrieving the current administrator password as taught by Cromer (¶[0021]). Lin further discloses determining the product serial number (Challener, col. 6, lines 16-17), of the BIOS ROM (col. 5, lines 55-57), in a case that the user password is set up (Challener, fig. 4, #503); and storing an added check sum value that is calculated by byte-adding the user password and the product serial number in a memory when the product serial number is not a default value in manufacturing (col. 8, lines 33-37 & col. 6, lines 13-17 and fig. 5, #607).

Regarding claim 3, Lin further discloses comprising: setting up a memory-mapped input/output region assigned as a BIOS writing protection region of a chipset having a GPIO (General Purpose Input Output) function as an input/output trap region and enabling an input/output trap (col. 2, lines 18-27).

Regarding claim 4, Lin lacks or does not expressly disclose storing the checksum in RAM or NVRAM. However, Challener further discloses wherein the storing the added check sum value (Lin, col. 6, line 20-23) in the memory comprises: storing the added check sum value in a CMOS RAM or a PNP NVRAM (col. 6, lines 12-15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Lin with the device of Challener to store the checksum in NVRAM in order to retain the stored checksum, as taught by Challener (col. 6, lines 12-15).

9. Claims 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Challener as applied to claim 5 above, and further in view of Freeman et al., US Publication No. 2004/003265.

Regarding claims 8-10, Lin further discloses wherein the allowing of the event disabling of the BIOS writing protection to occur comprises allowing the input/output trap to occur (fig. 3, #202 and #206). Lin lacks or does not expressly disclose allowing writing to the BIOS ROM by a PNP NVRAM (Plug And Play Non-Volatile Random Access Memory) manager to occur. However, Freeman discloses allowing writing to the BIOS ROM by a PNP NVRAM (Plug And Play Non-Volatile Random Access Memory) manager to occur (¶[0009]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Lin with the device of Freeman to utilize a PNP NVRAM in order to write to the BIO ROM as taught by Freeman (¶[0009]).

Regarding claim 12 Lin lacks or does not expressly disclose displaying an error message. However Challener discloses displaying an error message when the product serial number is a default value in manufacturing, or when the check sum values (Lin, col. 6, lines 20-23) are not equal (fig. 4, #517). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Lin with the device of Challener to display an error message when the checksums do not match in order to notify the user the access in invalid, as taught by Challener (fig. 4, #517).

10. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Freeman, U.S. Patent Application Publication Number 2004/0003265, in view of Challener and in further view of Lin.

Regarding claim 14, Freeman discloses method of improving BIOS (Basic Input Output System) security of a computer system (abstract), comprising: receiving an inputted password (fig. 2, #203); and enabling writing to a BIOS ROM. Freeman lacks determining if a stored and calculated check sum values based on inputted password are equal. However, Lin discloses having a security maintenance structure, when a stored check sum value and a calculated check sum value based upon the inputted password (Freeman, fig. 2, #204 and #210) are equal (col. 6, lines 53-57).
It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Freeman with the device of Lin to compare a stored

and calculated check sum value in order to further verify that writing to the BIOS is secure as taught by Lin (col. 6, lines 20-23). Freeman further discloses wherein the security maintenance structure of the BIOS ROM is not changed (fig. 2, #209).

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aubrey H. Wyszynski whose telephone number is (571)272-8155. The examiner can normally be reached on Monday - Thursday, and alternate Friday's.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on (571)272-3799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AHW

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